IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Gilbert Wolrich et al.	Art Unit	: 2183
Serial No.	: 10/069,352	Examiner	: David J. Huisman
Filed	: August 7, 2002	Conf. No.	: 7931
Title	: FAST WRITE INSTRUCTION FOR MICRO ENGINE USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, Applicant responds to the Examiner's Answer as follows.

Claim 1

The examiner states:

> **...Bhattacharya is concerned with how a result is written to a register and how a result is forwarded to a subsequent instruction. These are mutually exclusive operations. The claims focus on the former concept of how a result is written to a register. Hence, this is the focus of the examiner in making his rejection. However, Appellant's arguments are related to the latter concept of how forwarding is performed and not how a result is written to a result register. The examiner asserts that this examination is concerned with how the result is written, and not what is done with the result after it is written, and consequently appellant's arguments are non-effective. Specifically, appellant argues that the claim is not anticipated because, in Bhattacharya, "the instructions in the source register and the data in the results register are mapped by binding values in a logic circuit." While the examiner asserts that this is true, this has nothing to do with selecting bits in a result register and writing a result to those bits.**

Appellant contends that the examiner has missed the point of the argument laid out in the Appellant's Appeal Brief filed March 10, 2008. Specifically, the examiner has made no reference to a "fast-write instruction" as recited in claim 1 in his argument *supra*. Appellant's argument was that the binding values in the logic circuit of Bhattacharya teach away from the fast-write instruction of claim 1. In fact, nowhere in the examiner's argument regarding claim 1 is the concept of a fast-write instruction ever mentioned.

The examiner also states:

> **…in order to distinguish between threads, they must each be uniquely identifiable, and therefore include thread numbers. As a side note, it should be further realized that there is no requirement in the claim that a physical thread number be stored anywhere within a processor. That is, there is nothing stopping a person from simply assigning thread numbers mentally and realizing that the processor selects a register section based on that mental assignment.**

Appellant reminds the Board that the rejection of claim 1 is under 35 U.S.C. § 102(b). The examiner appears to argue that he need not consider the limitation by stating that "**nothing stopping a person from simply assigning thread numbers mentally.**" All of the feature of claim 1 must be considered. The examiner ignores the claim features that claim 1 is directed to " a method of operating a multi-threaded processor" and includes the feature of: "receiving data specified by execution of a fast-write instruction in one of multiple threads processing on the multi-threaded processor, the one of the multiple threads identified by a processing thread number … ." Therefore by the plain, reasonable construction given to claim 1, the claim cannot read on "**assigning thread numbers mentally.**" Therefore, the fact remains that Bhattacharya neither describes nor suggests at least the features of "selecting a group of bits associated with the one of the multiple threads, the group of bits being selected from...multiple groups of bits of [a] register specified by [a] fast-write instruction according to [a] processing thread number," and the examiner must consider the limitation.

Claim 2

The examiner states: "**It appears that appellant doesn't have an issue with the examiner's explanation of how the register is a control and status register. Instead, appellant argues that even if it were a control and status register, it isn't specified by a fast-write instruction.**" Footnote 18 on Page 11 of Appellant's Appeal Brief filed March 10, 2008 states that "**Appellant does not concede that [the register of Bhattacharya is a control and status register] is the case.**" The examiner is reminded that the meaning of "*arguendo*" is "for the sake of argument."

The examiner also states: "**…in Bhattacharya, an instruction specifies at least one register of a number of registers to store the result of the instruction. See column 2, lines 37-43, and column 3, lines 6-8, of Bhattacharya, and Sproull, page 49, column 1, section "Basic Structure", paragraph 2. Therefore, a result register is clearly specified by an instruction.**" Appellant has argued that, in the places referenced by the examiner, Bhattacharya's instructions carry a binding value through which a register is

associated. That is, the instruction of Bhattacharya does not specify the register. Further, to repeat, Appellant never conceded that the "results register" of Bhattacharya is a control and status register, as recited in claim 2.

Claim 6

The examiner states:

> **The examiner has been unable to find an explicit definition of micro-engine in the specification that would distinguish it from any general component that simply processes threads in Bhattacharya. The examiner pointed out that the pipeline of Fig.5 is a micro-engine. It contains multiple program counters and micro-sequencers, and all the logic necessary to execute threads. Hence, this is a micro-engine.**

Appellant reminds the Board that claim 6 recites "...the one of the multiple threads is processed on a micro engine of a multi-threaded processor." The pipeline of FIG. 5 of Bhattacharya are not micro engines that process threads but rather contain, as the examiner points out, program counters and micro-sequencers that "...**provide address designations in succeeding pipeline stages for both the result values flowing in the result pipeline and the instructions flowing in the instruction pipeline.**"

For these reasons, and the reasons stated in the Appeal Brief, Applicant submits that the final rejection should be reversed.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 5, 2008

/Denis G. Maloney/
Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906